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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,765	11/07/2001	Franck Roche	00RO30454288	9186

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
09/16/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

creganoa@addmg.com

Office Action Summary	Application No.	Applicant(s)	
	10/039,765	ROCHE ET AL.	
	Examiner	Art Unit	
	NIMESH G. PATEL	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20,24,28,31,32,36,40,43 and 48-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20,24,28,31,32,36,40,43 and 48-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on July 13, 2010 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 20, 24, 28, 31, 32, 36, 40, 43 and 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over SPI Block Guide(hereinafter referred to as SPI), in view of System Management Bus (SMBus) Specification(hereinafter referred to as SMB).

4. Regarding claim 20, SPI discloses a method of transmitting data between a master device and a slave device via a clock line and at least one data line, the clock line being maintained by default on a first logic value(SCK=1), the method comprising: providing the master device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value(Page 27, Figure 4-2, SCK=0 at SCK Edge Nr. 1); tying the clock line to the second logic value, via the master device, after data is applied to the data line(Figure

4-2, Data is applied before SCK Edge Nr. 1); and maintaining the data on the data line by the second device of the master and slave devices sending the data(Figure 4-2, Data is applied until rising edge of clock).

SPI does not specifically disclose the slave device having the ability to tie the clock and maintaining the tie to the clock line by the device to which the data is sent and releasing the clock. However, SMB discloses maintaining the tie to the clock line by the by the device to which the data is sent(Page 22, Section 4.3.3, Figure 4-7). It would have been obvious to one of ordinary skill in the art to have the device receiving data to hold the clock down, as disclosed by SMB, in the method of SPI, since this would allow clock synchronization to allow slower slave devices to cope with faster masters. The combination of SPI and SMB would implicitly maintain data on the data line by the sending device until an instant after the slave releases the clock line since the data changes only on clock transitions and the clock only transitions when the slave release the clock.

5. SPI and SMB further disclose the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device(SPI: Figure 4-2, Data is applied before SCK Edge Nr. 1), the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device(SMB: Section 4.3.3, Figure 4-7), wherein the master device ties the clock line to the second logic value when the master device receives data from the slave device and wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies data to the data line when the slave device is sending data to the master device(SPI: Figure 4-2; SMB: Section 4.3.3, Figure 4-7).

6. Regarding claim 24, SMB discloses a method wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line(Page 22, Section 4.3.3, Figure 4-7).

7. Regarding claim 28, SPI discloses a method wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device(Figure 4-2).

8. Regarding claim 31, SPI discloses a method, wherein the first logic value is 1 and the second logic value is 0(Figure 4-2).

9. Regarding claim 32, SPI discloses a method of transmitting data between a master device and a slave device via a clock line and at least one data line, the clock line being maintained by default on a first logic value(SCK=1), the method comprising: maintaining the clock line on a first logic value by default(SCK=1); providing the master device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value(Page 27, Figure 4-2, SCK=0 at SCK Edge Nr. 1); tying the clock line to the second logic value, via the master device, after data is applied to the data line(Figure 4-2, Data is applied before SCK Edge Nr. 1); and maintaining the data on the data line by the second device of the master and slave devices sending the data(Figure 4-2, Data is applied until rising edge of clock).

SPI does not specifically disclose the slave device having the ability to tie the clock and maintaining the tie to the clock line by the device to which the data is sent and releasing the clock. However, SMB discloses maintaining the tie to the clock line by the by the device to which the data is sent(Page 22, Section 4.3.3, Figure 4-7). It would have been obvious to one of ordinary skill in the art to have the device receiving data to hold the clock down, as disclosed by

SMB, in the method of SPI, since this would allow clock synchronization to allow slower slave devices to cope with faster masters. The combination of SPI and SMB would implicitly maintain data on the data line by the sending device until an instant after the slave releases the clock line since the data changes only on clock transitions and the clock only transitions when the slave release the clock.

10. SPI and SMB further disclose the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device(SPI: Figure 4-2, Data is applied before SCK Edge Nr. 1), the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device(SMB: Section 4.3.3, Figure 4-7), wherein the master device ties the clock line to the second logic value when the master device receives data from the slave device and wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies data to the data line when the slave device is sending data to the master device(SPI: Figure 4-2; SMB: Section 4.3.3, Figure 4-7).

11. Regarding claim 36, SMB discloses a method, wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line(Section 4.3.3, Figure 4-7).

12. Regarding claim 40, SPI discloses a method wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device(Figure 4-2).

13. Regarding claim 43, SPI discloses a method wherein the first logic value is 1 and the second logic value is 0(Figure 4-2).

14. Regarding claim 48, SPI discloses a synchronous data transmission system comprising: a clock line; a data line; a master data transmitting/receiving comprising a clock line connection terminal for connection to a clock line; at least one data line connection terminal for connection to a data line(page 27, Figure 4-2); a circuit for tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value(high)(Page 27, Figure 4-2, SCK changes from 1 to 0 at SCK Edge Nr. 1); and data sending unit for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value(Figure 4-2, Data is applied before SCK Edge Nr. 1), then releasing the clock line, and maintaining the data, when the data is to be sent(Figure 4-2) and a slave data transmitting/receiving comprising a clock line connection terminal connected to the clock line; at least one data line connection terminal connected to the data line and means for detecting a change from the first logic value to the second logic value on the clock line, and reading the data on the data line, when the data is to be received(Figure 4-2).

SPI does not specifically disclose maintaining the tie to the clock line by the device to which the data is sent and releasing the clock. However, SMB discloses maintaining the tie to the clock line by the by the device to which the data is sent(Page 22, Section 4.3.3, Figure 4-7). It would have been obvious to one of ordinary skill in the art to have the device receiving data to hold the clock down, as disclosed by SMB, in the method of SPI, since this would allow clock synchronization to allow slower slave devices to cope with faster masters. The combination of SPI and SMB would implicitly maintain data on the data line by the sending device until an instant after the slave releases the clock line since the data changes only on clock transitions and the clock only transitions when the slave release the clock.

15. SPI and SMB further disclose the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the

slave device(SPI: Figure 4-2, Data is applied before SCK Edge Nr. 1), the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device(SMB: Section 4.3.3, Figure 4-7), wherein the master device ties the clock line to the second logic value when the master device receives data from the slave device and wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies data to the data line when the slave device is sending data to the master device(SPI: Figure 4-2; SMB: Section 4.3.3, Figure 4-7).

16. Regarding claim 49, SPI discloses a system, wherein the master device further comprises data receiving unit for waiting for the clock line to have the first logic value(Figure 4-2).

17. Regarding claim 50, SMB discloses a system, wherein the slave device further comprises means for detecting a change from the first logic value to the second logic value on the clock line(Page 22, Section 4.3.3, Figure 4-7).

Response to Arguments

18. Applicant's arguments filed July 13, 2010 have been fully considered but they are not persuasive.

19. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The missing features in SPI, i.e. the slave tying the clock to the second logic value and releasing the clock is taught by SMB(Page 22).

20. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). It appears that applicant is arguing that SMB shows clock stretching during times when data is allowed to change. However, the main thing one of ordinary skill in the art would learn from SMB is to stretch the clock to allow slower devices to synchronize with faster devices. One of ordinary skill in the art would take that teaching and apply it to SPI, which works on a different protocol. So, it does not necessarily mean that one skilled in the art would stretch the clock when data is changing. In SPI, data transitions on the clock edges. Taking the clock stretching teaching by SMB, a device would be able to tie the clock down. And until the device releases the clock, the data will be valid and cannot change. Therefore the combination of SPI and SMB teach the clock being stretched if needed by holding the clock wire down and maintaining the data by the sender.

21. Therefore, applicant's arguments are not persuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIMESH G. PATEL whose telephone number is (571)272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rinehart H. Mark can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nimesh G Patel/
Examiner, Art Unit 2111

/Mark Rinehart/
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